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CORPORATION

DC-to-DC Voltage Converter

CLM7660

FEATURES

- **Converts +5V Logic Supply to ±5 System**
- **Wide Input Voltage Range . . . . . 1.5V to 10V**
- **Low Power Supply. 500µA**
- **Efficient Voltage Conversion 99.9%**
- **RS232 Negative Power Supply**
- **Low Cost, Simple to Use**

APPLICATIONS

- **A-to-D Converters**
- **D-to-A Converters**
- **Multiplexers**
- **Operational Amplifiers**

DESCRIPTION

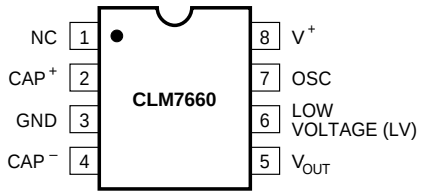
Calogic CLM7660 DC-to-DC converter will generate a negative voltage from a positive source. The CLM7660 generates -5V in +5V digital systems and with two external capacitors, the device will convert a 1.5V to 10V input signal to a -1.5V to -10V level.

Applications include analog-to-digital converters, digital-to-analog converters, operational amplifiers and multiplexers. Many of these systems require negative supply voltages. The CLM7660 allows +5V digital logic systems to incorporate these analog components without an additional main power source. Lower part count, less real estate, ease of use are just a few of the benefits of the CLM7660.

ORDERING INFORMATION

Part	Package	Temperature
CLM7660CP	8 Pin DIP	-40°C to +85°C
CLM7660DY	8 Pin SOIC	-40°C to +85°C

PIN CONFIGURATION AND BLOCK DIAGRAM



NC = NO INTERNAL CONNECTION

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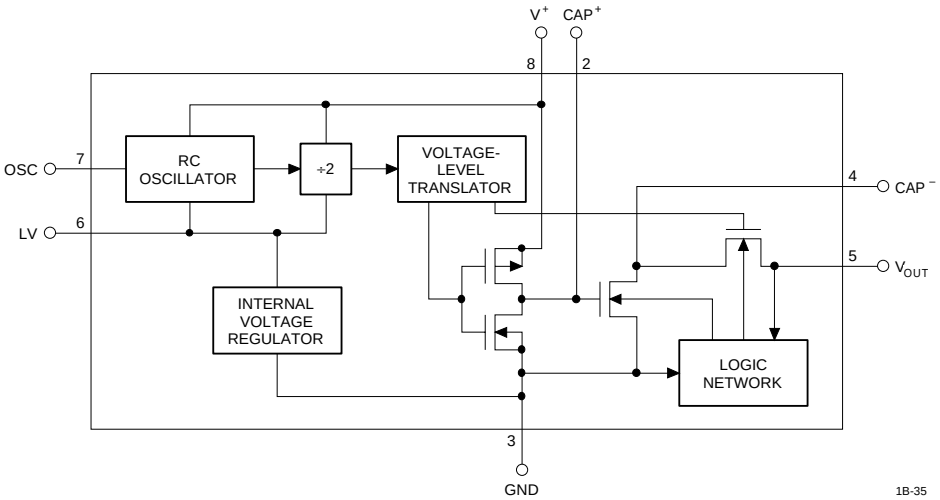

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calogic CORPORATION

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . +10.5V
LV and OSC Inputs
Voltage (Note 1) . . . . . -0.3V to (V^++0.3V)
for V^+ <5.5V
(V^+-5.5V) to (V^++0.3V)
for V^+ <5.5V
Current into LV (Note 1) . . . . . 20µA for V^+ >3.5V
Output Short Duration ($V_{SUPPLY} \leq 5.5V$) . . . . . Continuous
Power Dissipation (Note 2)
Plastic DIP 375mW

Operating Temperature Range
D Suffix . . . . . -40°C to +85°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS $V^+ = 5V$, $T_A = +25°C$, $C_{OSC} = 0$, Test Circuit (Figure 1), unless otherwise indicated.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
I^+	Supply Current	-	80	180	µA	$R_L = \infty$
V^+_{H1}	Supply Voltage Range, High	3	-	6.5	V	$0°C \leq T_A \leq +70°C$, R_L = 10kΩ, LV Open
		3	-	5	V	$-55°C \leq T_A \leq +125°C$, 10kΩ, LV Open
V^+_{L1}	Supply Voltage Range, Low (D_X Out of Circuit)	1.5	-	3.5	V	Min ≤ T_A ≤ Max, R_L = 10kΩ, LV to GND
V^+_{H2}	Supply Voltage Range, High (D_X In Circuit)	3	-	10	V	Min ≤ T_A ≤ Max, R_L = 10kΩ, LV Open
V^+_{L2}	Supply Voltage Range, Low (D_X In Circuit)	1.5	-	3.5	V	Min ≤ T_A ≤ Max, R_L = 10kΩ, LV to GND
R_{OUT}	Output Source Resistance	-	55	100	Ω	I_{OUT} = 20mA, $T_A = 25°C$
		-	-	120	Ω	I_{OUT} = 20mA, $0°C \leq T_A \leq +70°C$ (C Device)
		-	-	300	Ω	V^+ = 2V, I_{OUT} = 3mA, LV to GND $0°C \leq T_A \leq +70°C$
f_{OSC}	Oscillator Frequency	-	10	-	kHz	
PEF	Power Efficiency	95	98	-	%	R_L = 5kΩ
$V_{OUT\ EF}$	Voltage Conversion Efficiency	97	99.9	-	%	$R_L = \infty$
Z_{OSC}	Oscillator Impedance	-	1	-	MΩ	V^+ = 2V
		-	100	-	kΩ	V^+ = 5V

NOTES:
1. Connecting any input terminal to voltages greater than C+ or less than GND may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the CLM7660.
2. Derate linearly above 50°C by 5.5mW/°C.

CIRCUIT DESCRIPTION

The CLM7660 is an excellent voltage doubler, the device has all the characteristic with the exception of two inexpensive 10μF polarized electrolytic external capacitors. Figure 3 demonstrates the most effective means of using the device as a voltage doubler. Capacitor C_1 is charged to a voltage, V+, for the half cycle when switches S_1 and S_3 are closed. (Note Switches S_2 and S_4 are open during this half cycle.) During the second half of the operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V+ volts. Charge is then transferred from C_1 to C_2, such that voltage on C_2 is exactly V+, asumming ideal switches and no load on C_2.

The four switches in Figure 3 are MOS power switches, S_1 is a P-Channel device, S_2, S_3 and S_4 are N-Channel devices. The major challenge with this approach while integrating the switches, the substrates of S_3 and S_4 must always remain reversed-biased with respect to their sources, but not so much as to degrade their ON-resistances. In addition, at circuit start-up, and under short circuit conditions ($V_{OUT}=V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this will result in high power losses and probable device latch-up.

The above problem is eliminated in the CLM7660 by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 and S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the CLM7660 is an integral part of the anti-latch-up circuitry. Its inherent voltage drop can degrade operation at low voltages. To improve low-voltage operation, the LV pin should be connected to GND, disabling the regulator. For supply voltages greater than 3.5V, the LV terminal must be left open to ensure latch-up proof operation and prevent device damage.

THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory, a voltage multiplier can approach 100% efficiency if certain conditions are met:

1. The drive circuitry consumes minimal power.
2. The output switches have extremely low ON-resistance and virtually no offset.
3. The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

When larger values of C_1 and C_2 are used, the CLM7660 approaches the above conditions for negative voltage multiplication. Energy is lost only if the transfer of the charge between capacitors if a change in voltage occurs. The energy lost is defined by:

$E=1/2C_1 (V_12-V_22)$

During the pump and transfer cycles V_1 and V_2 are the voltages on C_1. If the impedances of C_1 and C_2 are high at the pump frequency (see Figure 3), compared to the value of R_L, there will be a substantial difference in voltages V_1 and V_2. The most optimum selection would be to make C_2 as large as possible to eliminate output voltage ripple, and to utilize a large value for C_1 to achieve maximum efficiency of operation.

OPERATIONAL RULES:

Never exceed maximum supply voltages.

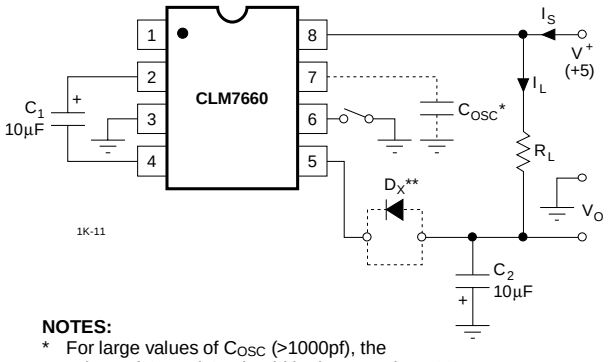
Never connect LV terminal to GND for supply voltages over 3.5V.

Never short circuit the output to V^+ supply voltages above 5.5V for extended periods; however, transient conditions including start-up are acceptable.

For polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the CLM7660 and the + terminal to of C_2 must be connected to GND.

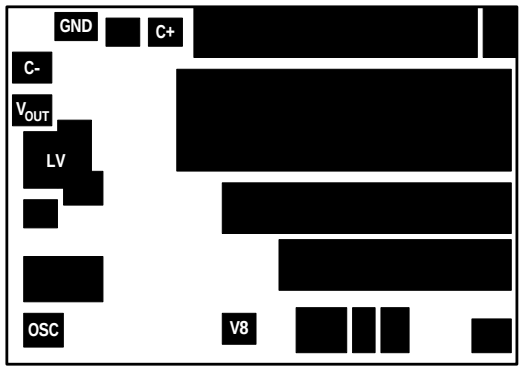
For high-voltage, elevated temperature applications add a diode D_X (reference Figure 1). The 1N914 diode is an appropriate choice.

FIGURE 1. CLM7660 TEST CIRCUIT



NOTES:
* For large values of C_{OSC} (>1000pf), the values of C_1 and C_2 should be increased to 100µF.
** DX is required for supply voltages greater than 6.5V at $-55^o \le T_A \le +70^oC$. Refer to performance curves for additional information.

FIGURE 2. CHIP TOPOGRAPHY



DIE SIZE = 81.5 x 57.5 (mm)

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FIGURE 3. IDEALIZED SWITCHED CAPACITOR

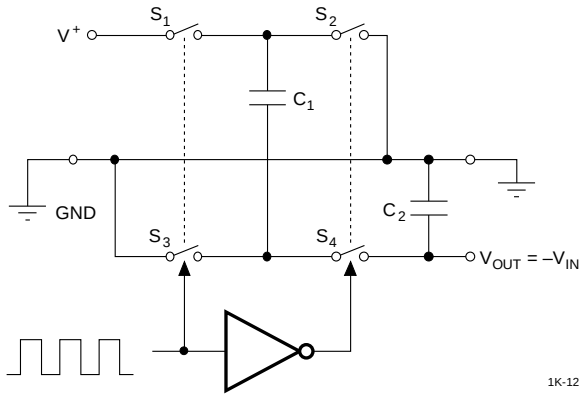
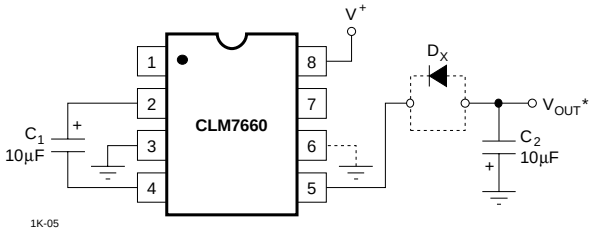


FIGURE 4. SIMPLE NEGATIVE CONVERTER



***NOTES:**
1. $V_{OUT} = -n\ V^+$ for $1.5V \le V^+ \le 6.5V$.
2. $V_{OUT} = -n\ (V^+ - V_{FDX})$ for $6.5V \le V^+ \le 10V$.

FIGURE 5. PARALLELING DEVICES LOWERS OUTPUT IMPEDANCE

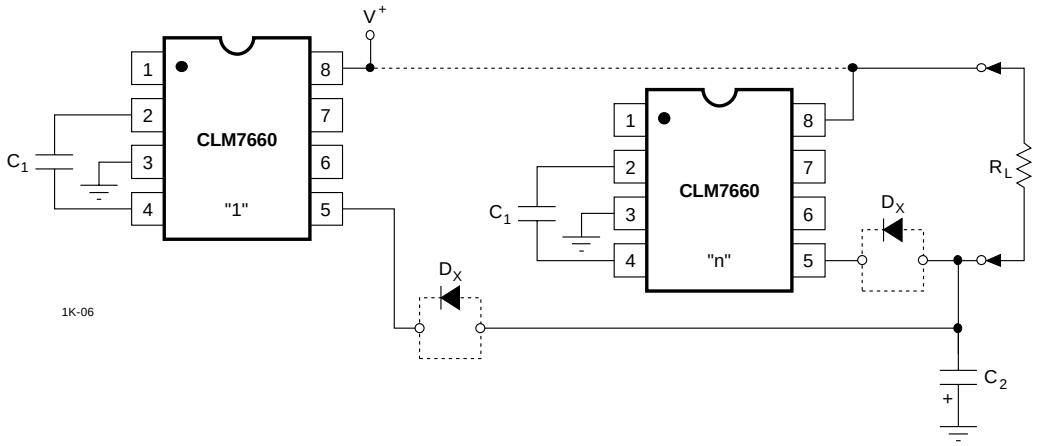
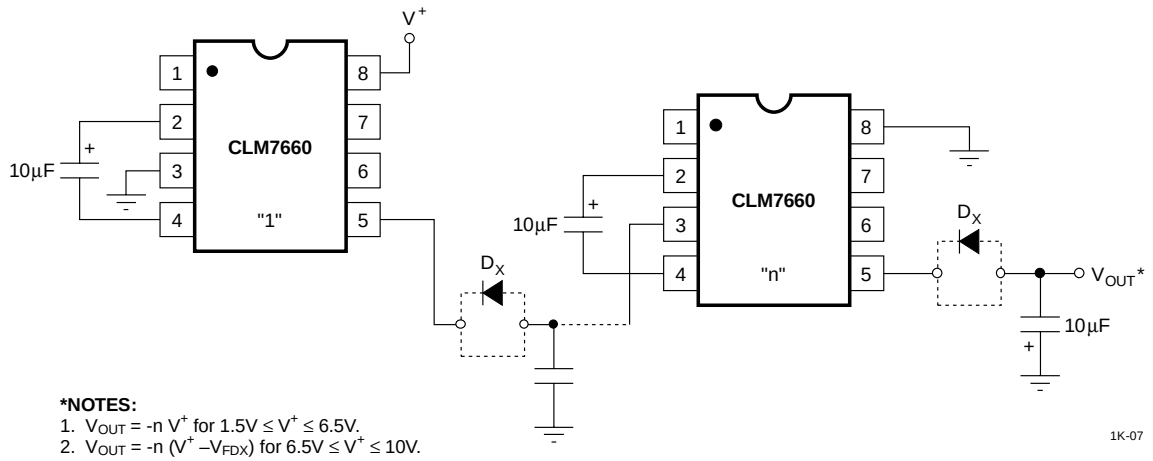


FIGURE 6. INCREASED OUTPUT VOLTAGE BY CASCADING DEVICES



***NOTES:**
1. $V_{OUT} = -n\ V^+$ for $1.5V \le V^+ \le 6.5V$.
2. $V_{OUT} = -n\ (V^+ - V_{FDX})$ for $6.5V \le V^+ \le 10V$.

FIGURE 7. EXTERNAL CLOCKING

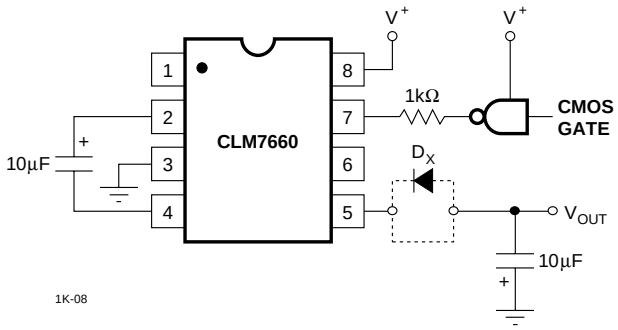


FIGURE 8. LOWERING OSCILLATOR FREQUENCY

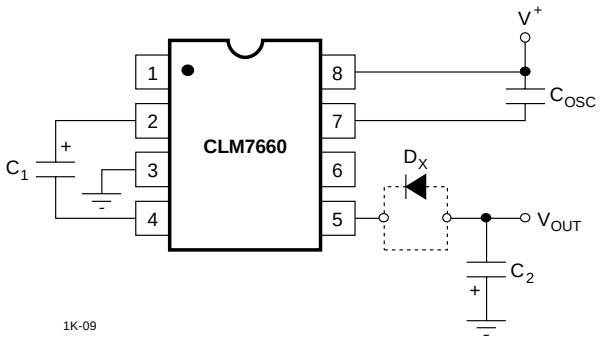


FIGURE 9. POSITIVE VOLTAGE MULTIPLIER

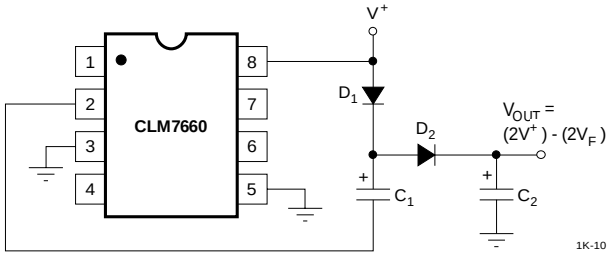


FIGURE 10. COMBINED NEGATIVE CONVERTER AND POSITIVE MULTIPLIER

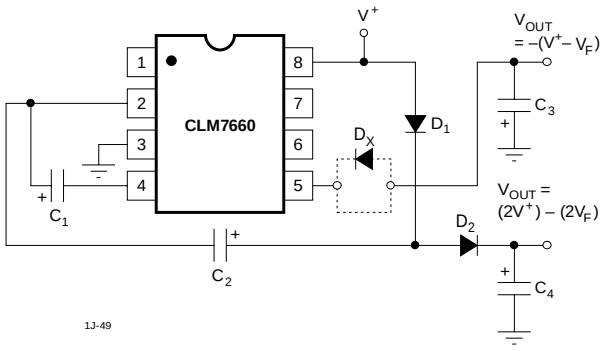


FIGURE 11. POSITIVE VOLTAGE CONVERSION

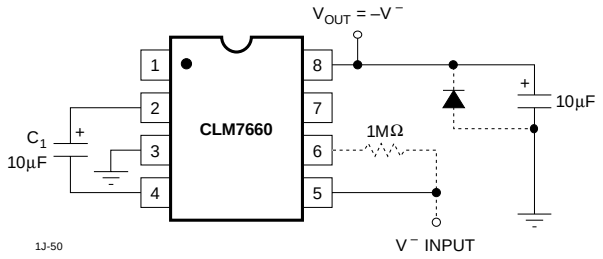


FIGURE 12. SPLITTING A SUPPLY IN HALF

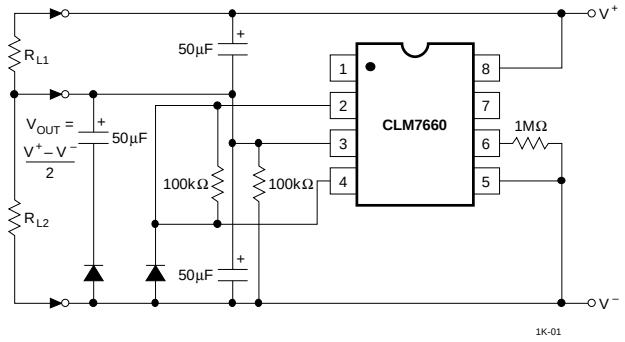


FIGURE 13A. FIXED POWER SUPPLY OPERATION OF CLM7106 A-D

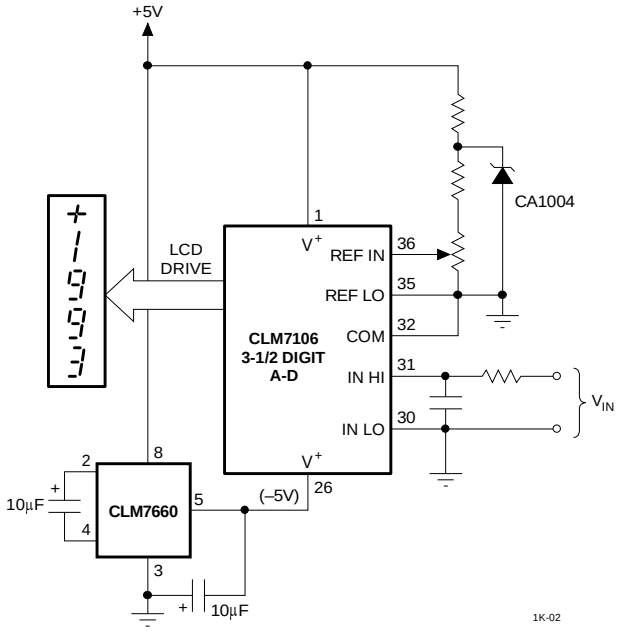


FIGURE 13B. NEGATIVE POWER SUPPLY GENERATION FOR 3 1/2 DIGIT A-D

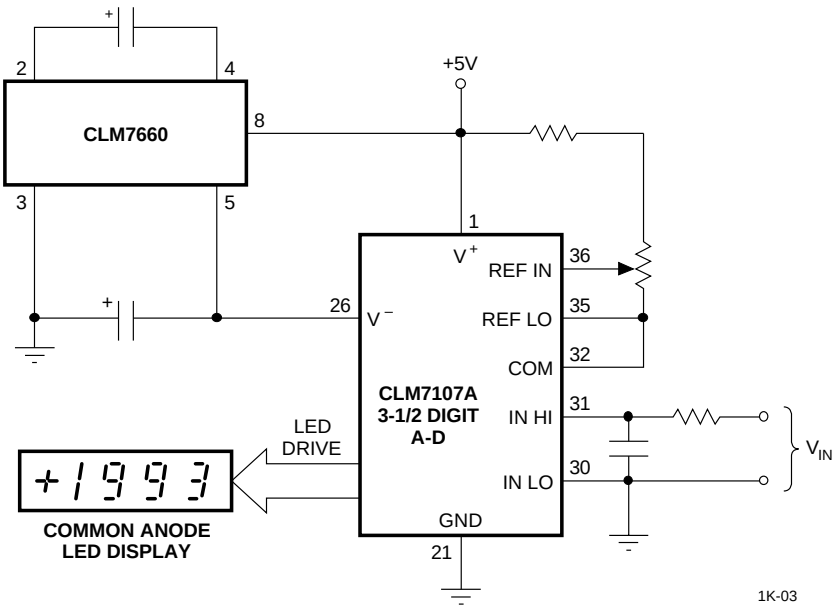
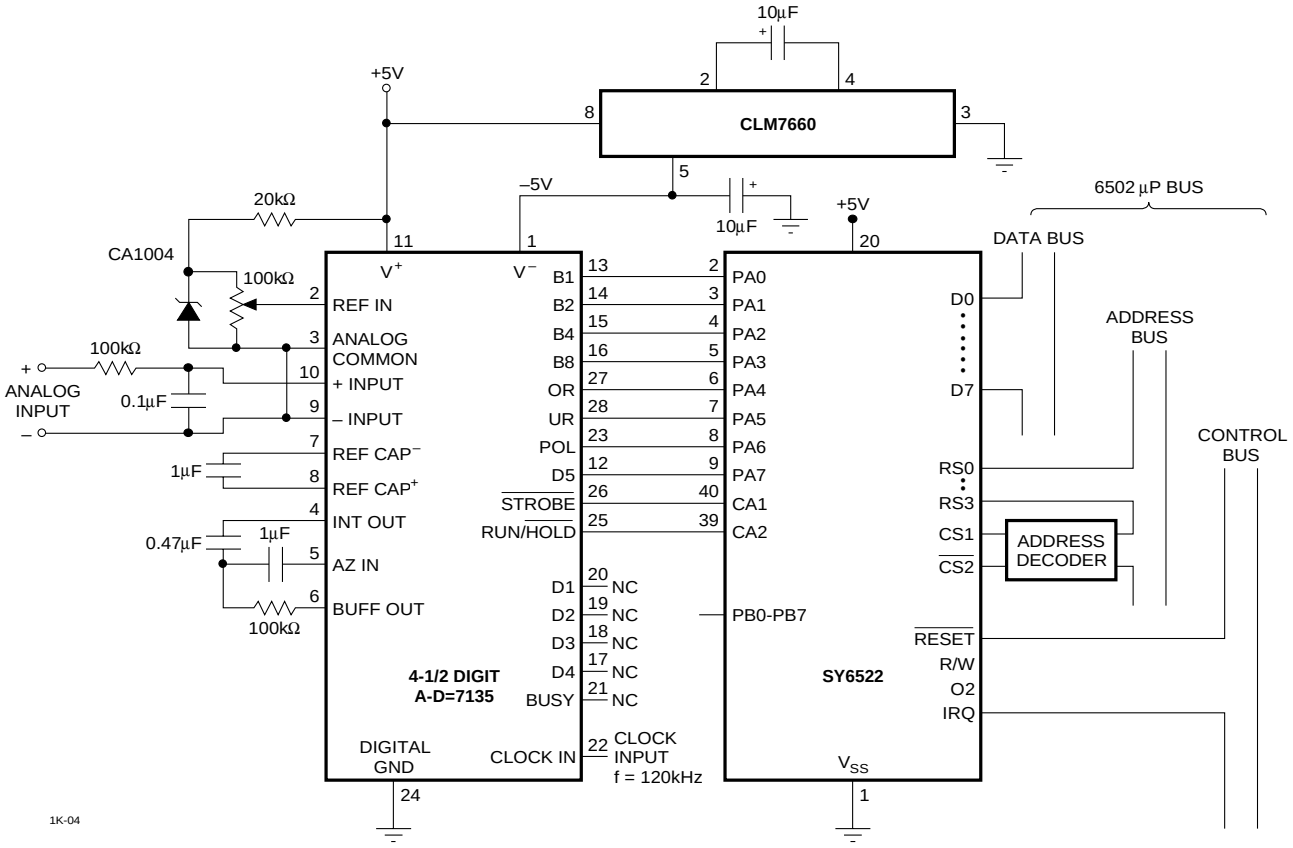
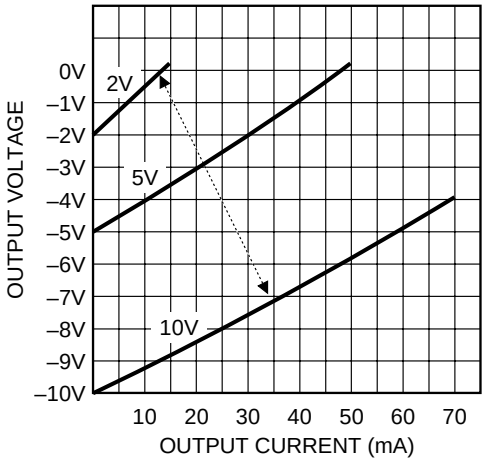


FIGURE 14. CLM7660 SUPPLIES -5V FOR CONVERTERS IN MICROPROCESSOR-CONTROLLED DATA ACQUISITION SYSTEMS



PERFORMANCE CURVES

OUTPUT VOLTAGE vs OUTPUT CURRENT



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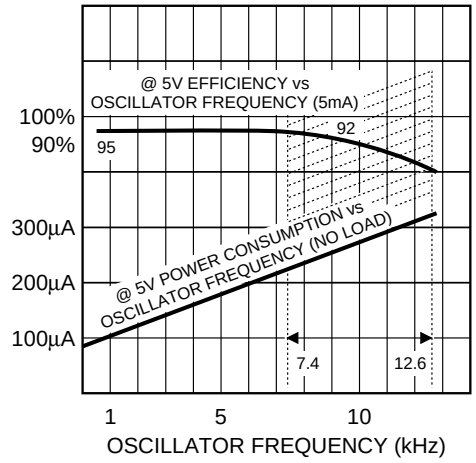

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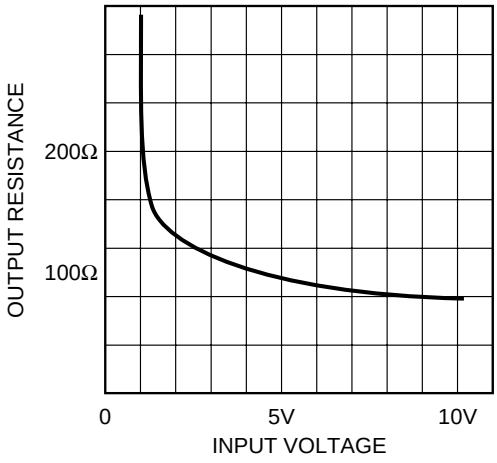
OUTPUT RESISTANCE vs SUPPLY VOLTAGE



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